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EXAMINER
DINH, PAUL

ART UNIT	PAPER NUMBER
2825	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/581,800	LAVELLE, EVAN MACKENZIE	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/24/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the application filed on 6/1/06.

Claims 1-18 are canceled

Claims 19-37 are pending.

Claim Objections

Claim 19 is objected to because:

A. As the claim presented, it is unclear and incomplete as to what "representation of the processor specification" represents and what "representation of the processor design" represents;

B. As the claim presented, it is unclear and incomplete regarding what/where the "instruction sequence" comes from; and

C. "a representation of the processor specification" and "a representation of the processor design" in claim 19 are not clearly described in the disclosure. See 37 CFR 1.75 (d).

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:
Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 19-37 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 19-37 are non-statutory because a § 101 process claim must (1) be tied to another statutory class (a particular machine or apparatus) or (2) transform underlying subject matter (such as an article or materials) to a different state or thing; see In Re Bilski, 545 F.3d 943, 88 USPQ2d 1385 (Fed. Cir. 2008). If neither of these requirements are met by the claim, the method is not a patent eligible process under § 101.

A § 101 process claim that would not qualify as a statutory process would be a claim that recites purely mental step(s) that can be performed manually or merely manipulating an abstract idea without the use of a specific structure. Thus, to qualify as a § 101 statutory process, the claimed step(s) must explicitly recite the other statutory class, i.e., the computer, the structure, the equipment, the thing, to which it is tied, for example by identifying the computer, the structure that accomplishes the step(s) and providing transformation underlying subject matter to a different state or thing.

Claim 19 recites a series of process steps for verification of a processor design including executing an instruction sequence in a first and a second simulation processes, but the steps neither explicitly recite a specific computer/structure/equipment that implement the claimed steps nor identify transformation of underlying subject matter to a different state or thing. Thus, the subject matter of claim 19 is non-statutory and not patent eligible.

Claims 20-37 are rejected because they depend directly or indirectly from claim 19.

In order to comply with the 35 USC § 101 statutory requirement, a limitation, ", by using a computer," or ", by a computer," must be inserted in at least one of the claimed steps of claim 19. This could be a tie and could overcome the 35 USC § 101 non-statutory issue.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 24 is rejected because the phrase "**may**" renders the claim indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Claims 25-26 are rejected because they depend from claim 24.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form The basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 19-37 are rejected under 35 U.S.C. 102(e) as being anticipated by the prior art of record Smith (US pub. 20050108501), Smith discloses:

(Claim 1)

A method of verifying a processor design against a processor specification (par 1-2), the method comprising:

a) Creating a verification environment *(see at least par 8*: "*FIG. 1 is a block diagram of an exemplary system for verifying processor architecture*");

b) Executing an instruction sequence in a first simulation process within the verification environment *(RTL simulator 12 in fig 1)*, the first simulation process comprising the execution of the instruction sequence according to a representation of the processor specification

(*Test case 10 in fig 1 includes test program, executable instructions, and instruction sequence according to a representation of the processor specification, representation of the processor specification is discloses in at least par 1, i.e., ., "program the desired architecture for the processor using a register transfer language (RTL). The desired architecture is represented by an RTL specification that describes the behavior of the processor…. The RTL specification models what the processor …, the processor architecture can be verified at a high level with reference to the RTL specification… The RTL specification also facilitates later hardware design of the processor)*

c) Executing the instruction sequence *(from test case 10)* in a second simulation process *(Golden simulator 14 in fig 1)*, the second simulation process comprising the execution of the instruction sequence according to a representation of the processor design (*i.e., at least par 20 discloses: " golden simulator 14 may be used in the design of more than one processor)*

d) Comparing results of the first simulation process with results of the second simulation process within the verification environment in order to verify the processor design (*Comparator 24 in fig 1 compares results of the first and simulation processes to verify the processor design*),

Wherein the representation of the processor specification is a machine-executable representation and the method further comprises processing the processor specification with a compiler to generate the machine-executable representation of the processor specification for the first simulation process (i.e., *one or more of the followings discloses this limitation:*

Par 2: "RTL specification (often compiled to increase speed)";

Par 17: "Referring to FIG. 1, a processor architecture verification system 1 is illustrated that verifies processor architecture by executing at least one test case 10 on both a register transfer language (RTL) simulator 12 that comprises a compiled version of the RTL specification, and a golden simulator 14 that comprises a relatively high-level program that emulates operation of the processor; and

Par 23: "the RTL specification may be implemented using any suitable tool for modeling the processor architecture 16, such as any register transfer language description of the architecture, which may be interpreted or compiled to act as a simulation of the processor")

(Claim 20) Wherein the processor specification comprises one or more verifiable elements (I.e., at least one of: circuit, behavior, architecture (par 1), operation, format (par 17), core, interface, states (par 23), timing, physical constraints (par 24), events, pipeline (par 26), path (par 41), packet (par 33-34), transactions (par 44), etc)

(Claim 21) wherein the verification environment maintains a current state of the one or more verifiable elements (see one or more of par: 22-23, 27-28, 30)

(Claim 22) wherein the processor specification further comprises at least one description of one or more instructions to be executed by the processor (see one or more of par: 1-2, 17-23).

(Claim 23) wherein each said at least one instruction description comprises **zero or more actions** associated with the instruction (*an instruction inherently comprises **zero or more** actions, for applicant information, this prior art discloses **zero or more actions** associated with the instruction, i.e., transaction, adding, removing, de-piping, depipeline, instructions acting on RTL simulator, activity, events, addition, modeling, changing, and **zero or more actions***

associated with the instruction from one or more of simulators, emulation, test case/program/instruction, etc, as disclosed in numerous location in this prior art)

(Claims 24-26) wherein the processor specification further comprises a description of a stimulus which may cause an exception condition in the processor (see above 112 rejection regarding may, one or more of simulators, emulation, test case/program/instruction may be a stimulus which may cause an exception condition in the processor) wherein said stimulus description comprises zero or more actions/entries associated with the stimulus (zero or more is inherent as detailed in claim 23)

(Claim 27) wherein each of the verifiable elements is associated with a respective specification queue (see at least one of stages, phases and pipeline in at least one of par 1, 21, 26, 29-30, 32), the method further comprising: executing actions associated with one or more instructions from the instruction sequence within the first simulation, wherein **zero or more** entries are added to the specification queue stimulus (zero or more is inherent as detailed in claim 23. For Applicant information, this prior art adds zero (nothing) **or** something, i.e., add/fill entries such as packet, paths, data, values from tables, transactions, etc)

(Claims 28-29) executing actions associated with a stimulus, wherein zero or more entries are added to a specification queue (zero or more is inherent as detailed in claim 23, for queue see at least one of stages, phases and pipeline in at least one of par 1, 21, 26, 29-30, 32. For Applicant information, this prior art adds zero (nothing) or something, i.e., add/fill entries such as packet, paths, data, values from tables, transactions, etc); wherein each of the verifiable elements is associated with a respective design queue (see at least one of stages, phases and pipeline in at least one of par 1, 21, 26, 29-30, 32)

(Claim 30) wherein the verification environment (shown in fig 1-2) receives one or more notifications from the second simulation (Golden Simulator), the one or more notifications being generated by the operation of the second simulation.

(Claim 31) the verification environment analyzing the one or more received notifications (fig 1-2); and the verification environment generating one or more entries in one or more design Queues (see at least one of stages, phases and pipeline in at least one of par 1, 21, 26, 29-30, 32) in response to the received notifications.

(Claim 32) wherein the processor specification comprises one or more verifiable elements (see claim 20 for one or more verifiable elements) for and each of the verifiable elements is associated with a respective specification queue (see at least one of stages, phases and pipeline in at least one of par 1, 21, 26, 29-30, 32), the method further comprising: executing actions associated with one or more instructions from the instruction sequence within the first simulation (RTL simulator) , wherein **zero or more** entries are added to the specification queue (zero or more is inherent as detailed in claim 23. For Applicant information, this prior art adds zero (nothing) or something, i.e., add/fill entries such as packet, data, paths, values from tables, transactions, etc; for queue see at least one of stages, phases and pipeline in at least one of par 1, 21, 26, 29-30, 32); and the verification environment verifying each verifiable element for which the design queue or the specification queue comprise one or more entries, by comparing (by the comparator shown in fig 1-2) the respective queues.

(Claim 33) wherein the verification environment (in fig 1-2) identifies reconcilable entries within each queue (see at least one of stages, phases and pipeline in at least one of par 1, 21, 26, 29-30, 32); and removes the reconcilable entries from the design queue and the specification queue and updates the state of the corresponding verifiable elements (see remove transactions in at least one of par 41, 53 and 55)

(Claim 34) wherein the verification environment reports an error if the design queue can not be reconciled with the compared specification queue (see at least one of: par 3, 6, 18, 27, and 53)

(Claims 35-36) wherein the verification environment:

Analyses the processor specification to determine a plurality of processor memory elements (see at least one of: fig 3-5);

Provides memory resources to the second simulation to implement the plurality of processor memory elements (see at least one of: fig 3-5)

(Claim 37) A computer-readable medium comprising code which, when executed causes a method according to claim 19 to be performed (see at least one of: par 58-61)

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, Jack Chiang can be reached on 571-272-7483. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Paul Dinh/
Primary Examiner, Art Unit 2825